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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Morgan *et al.* Art Unit: 2674

Serial No.: 09/088,674 Examiner: Nguyen, Kevin M.

Filed: 06/02/1998 Docket No. TI-25995

For: BOUNDARY DISPERSION FOR MITIGATING PWM TEMPORAL CONTOURING ARTIFACTS IN DIGITAL DISPLAYS

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NAME OF INVENTOR(S):	RECEIPT DATE & SERIAL NO.:
Morgan *et al.*	Application No.: 09/088,674
TITLE OF INVENTION: Boundary Dispersion for Mitigating PWM Temporal Contouring Artifacts in Digital Displays	**Filing Date:** 2 June 1998
TI FILE NO.: TI-25995 / DEPOSIT ACCT. NO.: **20-0668**	
FAXED: 11/15/2004 DUE: 11/14/2004 ATTY/SEC'Y: CAB:ss	

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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APPEAL BRIEF TRANSMITTAL

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8 November 2004

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Sir:

Transmitted herewith is an Appeal Brief in the above-identified application.

Please charge the $340.00 fee for filing the Brief to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Charge any additional fees, or credit overpayment to Deposit Account No. 20-0668.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Morgan

Art Unit: 2674

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Examiner: Nguyen, Kevin M.

Filed: 06/02/1998

Docket No. TI-25995

For: BOUNDARY DISPERSION FOR MITIGATING PWM TEMPORAL CONTOURING ARTIFACTS IN DIGITAL DISPLAYS

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

15 November 2004

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Charles A. Brill — 15 Nov. 2004

Charles A. Brill — Date

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed 14 June 2004, and the Advisory Action mailed 18 October 2004. Please charge all required fees, including any extension of time fees, to the deposit account of Texas Instruments Incorporated, Deposit Account No. 20-0668.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, to whom this application is assigned.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Applicant's legal representative.

STATUS OF THE CLAIMS

This application was filed on 2 June 1998 with ten claims, two of which were written in independent form. Claims 1-10 have been rejected and are under appeal herein.

STATUS OF THE AMENDMENTS

An amendment broadening the independent claims, Claim 1 and 6, was filed on 4 October 2000 and has been entered. Additional responses to final and non-final rejections were filed on 19 March 2001, 4 September 2001, 18 February 2002, 18 December 2002, 2 June 2003, 11 April 2004, and 12 August 2004 without amending any claims. Appeal Briefs were filed on 3 June 2002, and 4 August 2003.

SUMMARY OF CLAIMED SUBJECT MATTER

Line 22 of page 2 through line 16 of page 3 of the specification provides a concise explanation of the problem to be solved by the instant invention. Specifically, in real images, boundary conditions often exist where many display picture elements, or pixels, are spatially bunched together with similar image data. If the display system uses pulse width modulation (PWM) and the image data for the pixels has clusters of pixels that cross a major bit transition, PWM artifacts can occur.

The specification, from line 21 of page 3 through line 10 of page 5, provides a concise explanation of the invention defined in appealed independent Claim 1.

The present invention uses boundary dispersion to selectively offset nominal pixel values alternately between a positive offset and a negative offset, repeatedly over a sequence of displayed frames, whereby the average value of the two offset values over the displayed frames, as seen by the viewer, is equal to the nominal pixel value. For purpose of clarity the frame sequence described below refers to subsequent frames of source video data; however, the sequence can also be comprised of sub-frames within one frame of source video data. The chosen offset may be fixed, or may vary as a function of the nominal pixel value, the pixel spatial location on the screen, and pixel temporal location in time. The set of offsets applied to pixel values typically is varied over a repeating two-frame, or sub-frame, sequence. Selected offsets typically are applied to pixel values within each frame as a function of spatial location on the DMD, and which of the two-frames is being displayed. Within one frame, any given pixel value is offset by some amount above its correct value, and offset the same amount below its normal value in the next frame. Alternatively, the given pixel value is offset below its normal value in the first frame, and then offset above its normal value in the next frame. In either case, the average pixel value over the two-frames, as perceived by the viewer, is the nominal pixel value. The same is true of all pixels displayed on the DMD where an offset is used.

Boundary dispersion offsets certain pixel values from their nominal values in each frame according to preplanned spatial patterns. The spatial pattern used typically is dependent upon the value of the pixel codes. In each spatial pattern, some pixel values get a positive offset and some get a negative offset. In the next frame, an inverse set of

offsets are used so that all pixels average to their nominal values over the consecutive two-frame sequence.

A cluster of pixel codes at or near the transition of a major bit (e.g. 8, 16, 32, 64, 128 LSBs) use the offsets so that some pixels have a major bit set, and some without. Adjacent clusters of pixels, where one cluster contains pixels below the major bit and others contain pixels above the major bit, have the bit transition boundary dispersed. PWM contouring reduction is the result. The offsetting of some pixels positive and some negative in any given frame according to the spatial pattern also prevents any potential flicker artifacts that may be introduced by offsetting pixel codes over two frames.

A checkerboard pattern for a two-frame sequence is one predefined pattern used to a disperse bit transition spatially around a bit transition boundary, for instance, the bit B5, which corresponds to the value of 32. Areas of the screen around this bit transition, for instance, codes 26 through 29, use more complex two-frame patterns. The added complexity of these patterns is needed to control the density of pixels that have a major bit, e.g. B5, set in any given frame. A balance is struck between reducing PWM boundary artifacts and new artifacts introduced within a spatial area having a given code. This is because if to many (or to few) pixels have the major bits set, within an area using a given code, temporal noise can result in this area. The patterns are properly defined so that the contouring artifacts within a code (intra-code) are much less objectionable than the major bit transition boundaries (inter-code boundaries). By use of a particular pattern, for instance the checkerboard pattern, the spatial patterns have pixels with and without the major bits set are packed so spatially tightly that the intra-code contouring is not resolvable by a viewer at normal viewing distance. Since the PWM contouring is

dispersed over a larger area, the overall temporal artifacts seen in the image are greatly reduced.

The specification, on lines 4-29 of page 13, and referencing Figure 4, provides a concise explanation of the invention defined in appealed independent Claim 6.

A degamma function 30 is applied to each RGB color so that the DMD display output matches a CRT response. Since the degamma output is limited to 24 bits, a spatial contouring filter is included that diffuses the 8-bit per color quantization errors for low intensity pixels. The boundary dispersion logic 32 according to the present invention accepts the spatial contouring filter output. The boundary dispersion logic 32 receives signals to identify pixels spatially on the DMD, which signals are provided on signal lines row count ROWCNT and column count COLUMNCNT. A signal is also provided to identify the particular frame of the two-frame temporal sequence, identified as signal FRAME 1/2. A logic high on this line indicates a FRAME 1, and a logic 0 indicates FRAME 2. The boundary dispersion logic assigns spatial patterns as a function of these signals where offsets are applied to each 8-bit color pixel. The offset values are provided to the boundary dispersion logic 32 so that the correct offset is added or subtracted to each pixel in a particular spatial-temporal assignment, as shown in Figure 2 and illustrated in Table 1. The offsets and spatial-temporal patterns applied by the boundary dispersion logic 32 are also a function of the pixel codes. Table 1 illustrates this. Figure 2 illustrates how the boundary dispersion logic is applied to pixels in a spatial-temporal manner.

The 24 signals from the boundary dispersion logic 32 are input into the DMD data formatting logic 40. The DMD data formatting logic organizes the input data into words

which form digital planes of information and then loads them into banks of RAM 42. Data is written to one bank of RAM 40 while the other bank is being continuously read and written to the DMD. Thus, a double-buffer memory is used. The buffers are swapped at each VSYNC which indicates a frame boundary for source pixels.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether Claims 1-10 are anticipated under 35 U.S.C. § 102 (e) by U.S. Patent No. 6,222,515 to Yamaguchi *et al.*

ARGUMENT

Ground of Rejection 1:

Claims 1-10 were rejected under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 6,222,515 to Yamaguchi *et al.* ("Yamaguchi"). The applicant respectfully disagrees and submits the Examiner has failed to establish a prima facie case of anticipation under 35 U.S.C. § 102.

"A person shall be entitled to a patent unless," creates an initial presumption of patentability in favor of the applicant. 35 U.S.C. § 102. "We think the precise language of 35 U.S.C. § 102 that, "a person shall be entitled to a patent unless," concerning novelty and unobviousness, clearly places a burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103, see Graham and Adams." *In re Warner*, 379 F.2d 1011, 1016 (C.C.P.A. 1967) (referencing *Graham v. John Deere Co.*, 383 U.S. 1 (1966) and *United States v. Adams*, 383 U.S. 39 (1966)). "As adapted to *ex parte* procedure, *Graham* is interpreted as continuing to place the 'burden of proof on the Patent Office which requires it to produce

the factual basis for its rejection of an application under sections 102 and 103'." *In re Piasecki*, 745 F.2d 1468 (Fed. Cir. 1984) (citing *In re Warner*, 379 F.2d at 1016).

> "The prima facie case is a procedural tool which, as used in patent examination (as by courts in general), means not only that the evidence of the prior art would reasonably allow the conclusion the examiner seeks, but also that the prior art compels such a conclusion if the applicant produces no evidence or argument to rebut it." *In re Spada*, 911 F.2d 705, 708 n.3 (Fed. Cir. 1990).

The applicant respectfully submits the Examiner has failed to meet the burden of proof required to establish a prima facie case of anticipation. Section 2131 of the Manual of Patent Examiner's Procedure provides:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053, (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim . . . . *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Claim 1:

With respect to independent Claim 1, the Examiner has failed to provide a prima facie case of anticipation because the Examiner failed to provide any teaching in Yamaguchi of "offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame;

and offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 1.

The Examiner stated, "As to claims 1 and 6, Yamaguchi et al teaches a system of displaying a digital video data associated with a method comprising a logic circuit offsetting a first pixel value a first predetermined amount (2V, 4V) to form a first offset pixel value, said logic circuit (4) also offsetting said first said pixel value by the opposite of said first predetermined amount (-2V, -4V) to form a second offset value; and display panel (19) displaying said first offset pixel value during a first display frame 'a positive frame' and displaying said second offset pixel value during a second display frame 'a negative frame', such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value 'said means effective voltage of (+/- 3V) is shown by hatching in figure 7B' (see figures 1A, 1B, 7B, column 5, lines 58-64 and column 8, lines 11-27)."

The Examiner has failed to make a reasonable attempt to read the teachings of the prior art onto the limitations of the claims presented and therefore has failed to establish a prima facie case of anticipation. For example, the Examiner has not stated what value in Yamaguchi is interpreted by the Examiner as a "first pixel value" and therefore the Examiner's attempts to read Yamaguchi onto the present claim flounder. Having not established a first pixel value, the Examiner states a first predetermined offset amount is (2V, 4V) and a second predetermined offset amount is (-2V, -4V). These each appear to the applicant to be two amounts and the Examiner offers no explanation or support for his

interpretation of Yamaguchi. The Examiner then states the average of said displayed first offset pixel value and said second offset pixel value is +/- 3V. The applicant respectfully submits, that if the Examiner is averaging 2V, 4V, -2V, and -4V the average would be 0 volts. The Examiner's interpretation of Yamaguchi clearly is unsupported by Yamaguchi and does not follow the clear teachings of Yamaguchi. For example, Yamaguchi states, "To realize a gray-scale level 3, 6 (V) is applied to the first field and 2 (V) to the second field to produce a mean effective voltage of 4 (V) for one frame." (col. 8, lines 23-25).

The Examiner has failed to point to any teaching in Yamaguchi that the pixel value of digital video data is offset. The Examiner merely points to teachings of Yamaguchi that drive a particular pixel with a two or more voltages in order that the combination of the various voltages will have the same effect as driving the pixel with the average of the various voltages. For example, one embodiment of Yamaguchi drives an LCD element with 4 volts and 2 volts to simulate driving the LCD element with 3 volts.

Thus, rather than showing, teaching, or even suggesting "offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 1, Yamaguchi appears to merely teach creating a method of creating additional gray scale levels by sequentially using combinations of voltage levels.

The passages cited by the Examiner simply do not support the Examiner's transformation of the teachings of Yamaguchi to the recited elements of Claim 1, nor is there any basis or suggestion in the prior art to support this novel interpretation of the prior art. The Examiner's rejection of Claim 1 is unsupported by the prior art, fails to establish a prima facie case of anticipation, and therefore should be withdrawn.

Claim 2:

Claim 2 depends from Claim 1 and should be deemed allowable for that reason and on its own merits. For the reasons argued above with respect to Claim 1, Yamaguchi does not show, teach, or suggest the limitations of Claim 1, much less the limitations of Claim 1 in combination with the additional limitations of Claim 2.

Claim 2 recites, "the value of said first predetermined amount is selected as a function of said first pixel value." The Examiner has failed to make a prima facie case of anticipation for this combination of limitations. The Examiner merely stated, "Yamaguchi et al teaches the system associated the method comprising the value of said first predetermined amount (2V, 4V) is selected by said logic circuit as a function 'average' of said first pixel value 'said means effective voltage of 3V' (see figures 1A, column 5, lines 58-64)." While it is far from clear what the Examiner means by this statement, it clearly falls short of the standard require by *Richardson* referenced above, that the prior art must show "The identical invention must be shown in as complete detail as contained in the . . . claim." The Examiner's rejection of Claim 2 is unsupported by the prior art, fails to establish a prima facie case of anticipation, and therefore should be withdrawn.

Claim 3:

Claim 3 depends from Claim 1 and should be deemed allowable for that reason and on its own merits. For the reasons argued above with respect to Claim 1, Yamaguchi does not show, teach, or suggest the limitations of Claim 1, much less the limitations of Claim 1 in combination with the additional limitations of Claim 3.

Claim 3 recites, "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed." The Examiner has failed to make a prima facie case of anticipation for this combination of limitations. The Examiner merely stated, "Yamaguchi et al teaches the system associated the method comprising said first offset pixel value (+/-2V, +/-4V) is greater than or less than said first pixel value (3V) as a function of 'average' of the spatial location that said first pixel value 'said means effective voltage of (+/-3V)' is to be displayed (see figures 1A, 7B, column 8, lines 11-27)." While it is far from clear what the Examiner means by this statement, it clearly falls short of the standard require by *Richardson* referenced above, that the prior art must show "The identical invention must be shown in as complete detail as contained in the . . . claim." The Examiner's rejection of Claim 3 is unsupported by the prior art, fails to establish a prima facie case of anticipation, and therefore should be withdrawn.

Claim 4:

Claim 4 depends from Claim 1 and should be deemed allowable for that reason and on its own merits. For the reasons argued above with respect to Claim 1, Yamaguchi does not show, teach, or suggest the limitations of Claim 1, much less the limitations of Claim 1 in combination with the additional limitations of Claim 4.

Claim 4 recites, "said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame." The Examiner has failed to make a prima facie case of anticipation for this combination of limitations. The Examiner merely stated, "Yamaguchi et al teaches the system associated the method comprising said pixel value are displayed using a plurality of weighted bit-planes 'a first field memory (13), a second field memory (14)', wherein said first pixel values close to a bit transition of said bit-planes (13, 14) are offset during said first display frame 'said positive frame' and said second frame 'said negative frame' (see figure 1B, column 6, lines 41-55)." While it is far from clear what the Examiner means by this statement, it clearly falls short of the standard require by *Richardson* referenced above, that the prior art must show "The identical invention must be shown in as complete detail as contained in the . . . claim." The Examiner's rejection of Claim 4 is unsupported by the prior art, fails to establish a prima facie case of anticipation, and therefore should be withdrawn.

Claim 6:

With respect to independent Claim 6, the Examiner has failed to provide a prima facie case of anticipation because the Examiner failed to provide any teaching in Yamaguchi of "a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such

that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 6.

The Examiner stated, "As to claims 1 and 6, Yamaguchi et al teaches a system of displaying a digital video data associated with a method comprising a logic circuit offsetting a first pixel value a first predetermined amount (2V, 4V) to form a first offset pixel value, said logic circuit (4) also offsetting said first said pixel value by the opposite of said first predetermined amount (-2V, -4V) to form a second offset value; and display panel (19) displaying said first offset pixel value during a first display frame 'a positive frame' and displaying said second offset pixel value during a second display frame 'a negative frame', such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value 'said means effective voltage of (+/- 3V) is shown by hatching in figure 7B' (see figures 1A, 1B, 7B, column 5, lines 58-64 and column 8, lines 11-27)."

The Examiner has failed to make a reasonable attempt to read the teachings of the prior art onto the limitations of the claims presented and therefore has failed to establish a prima facie case of anticipation. For example, the Examiner has not stated what value in Yamaguchi is interpreted by the Examiner as a "first pixel value" and therefore the Examiner's attempts to read Yamaguchi onto the present claim flounder. Having not established a first pixel value, the Examiner states a first predetermined offset amount is (2V, 4V) and a second predetermined offset amount is (-2V, -4V). These each appear to the applicant to be two amounts and the Examiner offers no explanation or support for his interpretation of Yamaguchi. The Examiner then states the average of said displayed first offset pixel value and said second offset pixel value is +/- 3V. The applicant respectfully

submits, that if the Examiner is averaging 2V, 4V, -2V, and -4V the average would be 0 volts. The Examiner's interpretation of Yamaguchi clearly is unsupported by Yamaguchi and does not follow the clear teachings of Yamaguchi. For example, Yamaguchi states, "To realize a gray-scale level 3, 6 (V) is applied to the first field and 2 (V) to the second field to produce a mean effective voltage of 4 (V) for one frame." (col. 8, lines 23-25).

The Examiner has failed to point to any teaching in Yamaguchi that the pixel value of digital video data is offset. The Examiner merely points to teachings of Yamaguchi that drive a particular pixel with a two or more voltages in order that the combination of the various voltages will have the same effect as driving the pixel with the average of the various voltages. For example, one embodiment of Yamaguchi drives an LCD element with 4 volts and 2 volts to simulate driving the LCD element with 3 volts.

Thus, rather than showing, teaching, or even suggesting "a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 6, Yamaguchi appears to merely teach creating a method of creating additional gray scale levels by sequentially using combinations of voltage levels.

The passages cited by the Examiner simply do not support the Examiner's transformation of the teachings of Yamaguchi to the recited elements of Claim 6, nor is

there any basis or suggestion in the prior art to support this novel interpretation of the prior art. The Examiner's rejection is unsupported by the prior art, fails to establish a prima facie case of anticipation, and therefore should be withdrawn.

Claim 7:

Claim 7 depends from Claim 6 and should be deemed allowable for that reason and on its own merits. For the reasons argued above with respect to Claim 6, Yamaguchi does not show, teach, or suggest the limitations of Claim 6, much less the limitations of Claim 6 in combination with the additional limitations of Claim 7.

Claim 7 recites, "the value of said first predetermined amount is selected by said logic circuit as a function of said first pixel value." The Examiner has failed to make a prima facie case of anticipation for this combination of limitations. The Examiner merely stated, "Yamaguchi et al teaches the system associated the method comprising the value of said first predetermined amount (2V, 4V) is selected by said logic circuit as a function 'average' of said first pixel value 'said means effective voltage of 3V' (see figures 1A, column 5, lines 58-64)." While it is far from clear what the Examiner means by this statement, it clearly falls short of the standard require by *Richardson* referenced above, that the prior art must show "The identical invention must be shown in as complete detail as contained in the . . . claim." The Examiner's rejection of Claim 7 is unsupported by the prior art, fails to establish a prima facie case of anticipation, and therefore should be withdrawn.

Claim 8:

Claim 8 depends from Claim 6 and should be deemed allowable for that reason and on its own merits. For the reasons argued above with respect to Claim 6, Yamaguchi does not show, teach, or suggest the limitations of Claim 6, much less the limitations of Claim 6 in combination with the additional limitations of Claim 8.

Claim 8 recites, "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed." The Examiner has failed to make a prima facie case of anticipation for this combination of limitations. The Examiner merely stated, "Yamaguchi et al teaches the system associated the method comprising said first offset pixel value (+/-2V, +/-4V) is greater than or less than said first pixel value (3V) as a function of 'average' of the spatial location that said first pixel value 'said means effective voltage of (+/-3V)' is to be displayed (see figures 1A, 7B, column 8, lines 11-27)." While it is far from clear what the Examiner means by this statement, it clearly falls short of the standard require by *Richardson* referenced above, that the prior art must show "The identical invention must be shown in as complete detail as contained in the . . . claim." The Examiner's rejection of Claim 8 is unsupported by the prior art, fails to establish a prima facie case of anticipation, and therefore should be withdrawn.

Claim 9:

Claim 9 depends from Claim 6 and should be deemed allowable for that reason and on its own merits. For the reasons argued above with respect to Claim 6, Yamaguchi does not show, teach, or suggest the limitations of Claim 6, much less the limitations of Claim 6 in combination with the additional limitations of Claim 9.

Claim 9 recites, "said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame." The Examiner has failed to make a prima facie case of anticipation for this combination of limitations. The Examiner merely stated, "Yamaguchi et al teaches the system associated the method comprising said pixel value are displayed using a plurality of weighted bit-planes 'a first field memory (13), a second field memory (14)', wherein said first pixel values close to a bit transition of said bit-planes (13, 14) are offset during said first display frame 'said positive frame' and said second frame 'said negative frame' (see figure 1B, column 6, lines 41-55)." While it is far from clear what the Examiner means by this statement, it clearly falls short of the standard require by *Richardson* referenced above, that the prior art must show "The identical invention must be shown in as complete detail as contained in the . . . claim." The Examiner's rejection of Claim 9 is unsupported by the prior art, fails to establish a prima facie case of anticipation, and therefore should be withdrawn.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-10 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Please charge any fees necessary in connection with the filing of this paper, including any necessary extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

Charles A. Brill
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CLAIMS APPENDIX

1. (Previously presented) A method of displaying digital video data comprising pixel values, said method comprising the steps of:

offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and

offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

2. (Original) The method as specified in Claim 1 wherein the value of said first predetermined amount is selected as a function of said first pixel value.

3. (Original) The method as specified in Claim 1 wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed.

4. (Original) The method as specified in Claim 1 wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame.

5. (Original) The method as specified in Claim 1 wherein said first display frame and said second display frame are consecutive.

6. (Previously presented) A system of displaying digital video data comprising pixel

values, comprising:

a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and

display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

7. (Original) The system as specified in Claim 6 wherein the value of said first predetermined amount is selected by said logic circuit as a function of said first pixel value.

8. (Original) The system as specified in Claim 6 wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed.

9. (Original) The system as specified in Claim 6 wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame.

10. (Original) The system as specified in Claim 6 wherein said first display frame and said second display frame are consecutive.